

# Digital Step Attenuator

75Ω DC-2000 MHz

15.5 dB, 0.5 dB Step

5 Bit, Parallel Control Interface, Single Positive Supply Voltage, +3V

## Product Features

- Single positive supply voltage, +3V
- Immune to latch up
- Excellent accuracy, 0.1 dB Typ
- Parallel control interface
- Low Insertion Loss
- High IP3, +52 dBm Typ
- Very low DC power consumption
- Excellent return loss, 20 dB Typ
- Small size 4.0 x 4.0 mm



**DAT-15575-PP+**

CASE STYLE: DG983-1

## Typical Applications

- Base Station Infrastructure
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- Wireless Local Loop
- UNII & Hiper LAN
- Power amplifier distortion canceling loops

### +RoHS Compliant

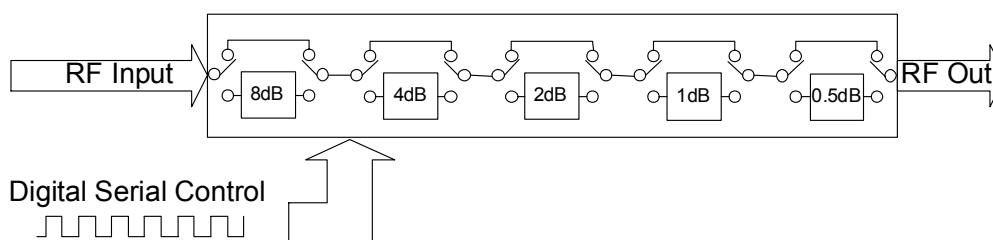
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

This model will be replaced in the future with a improved design. The new model will be [DAT-15575A-PP+](#). It will have similar performance, the same case style and footprint.

## General Description

The DAT-15575-PP+ is a 75Ω RF digital step attenuator that offers an attenuation range up to 15.5 dB in 0.5 dB steps. The control is a 5-bit parallel interface, operating on a single +3 volt supply. The DAT-15575-PP+ is produced using a unique CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

## Simplified Schematic



**RF Electrical Specifications, DC-2000 MHz,  $T_{AMB}=25^{\circ}\text{C}$ ,  $V_{DD}=+3\text{V}$** 

| Parameter                                                                          | Freq. Range (GHz) | Min. | Typ. | Max. | Units |
|------------------------------------------------------------------------------------|-------------------|------|------|------|-------|
| Accuracy @ 0.5 dB Attenuation Setting                                              | DC-1.2            | —    | 0.03 | 0.17 | dB    |
|                                                                                    | 1.2-2.0           | —    | 0.05 | 0.18 | dB    |
| Accuracy @ 1 dB Attenuation Setting                                                | DC-1.2            | —    | 0.03 | 0.19 | dB    |
|                                                                                    | 1.2-2.0           | —    | 0.1  | 0.2  | dB    |
| Accuracy @ 2 dB Attenuation Setting                                                | DC-1.2            | —    | 0.07 | 0.23 | dB    |
|                                                                                    | 1.2-2.0           | —    | 0.15 | 0.25 | dB    |
| Accuracy @ 4 dB Attenuation Setting                                                | DC-1.2            | —    | 0.05 | 0.25 | dB    |
|                                                                                    | 1.2-2.0           | —    | 0.15 | 0.35 | dB    |
| Accuracy @ 8 dB Attenuation Setting                                                | DC-1.2            | —    | 0.1  | 0.25 | dB    |
|                                                                                    | 1.2-2.0           | —    | 0.24 | 0.55 | dB    |
| Insertion Loss <sup>(note 1)</sup> @ all attenuator set to 0dB                     | DC-1.2            | —    | 1.2  | 1.8  | dB    |
|                                                                                    | 1.2-2.0           | —    | 1.6  | 2.1  | dB    |
| Input IP3 <sup>(note 2)</sup> (at Min. and Max. Attenuation)                       | DC-2.0            | —    | +52  | —    | dBm   |
| Input Power @ 0.2dB Compression <sup>(note 2)</sup> (at Min. and Max. Attenuation) | DC-2.0            | —    | +24  | —    | dBm   |
| VSWR                                                                               | DC-1.2            | —    | 1.6  | 2.0  | —     |
|                                                                                    | 1.2-2.0           | —    | 1.7  | 2.0  | —     |

**DC Electrical Specifications**

| Parameter                                                | Min.                | Typ. | Max.                | Units         |
|----------------------------------------------------------|---------------------|------|---------------------|---------------|
| $V_{DD}$ , Supply Voltage                                | 2.7                 | 3    | 3.3                 | V             |
| $I_{DD}$ , Supply Current, quiescent <sup>(note 3)</sup> | —                   | —    | 100                 | $\mu\text{A}$ |
| Control Input Low                                        | —                   | —    | $0.3 \times V_{DD}$ | V             |
| Control Input High                                       | $0.7 \times V_{DD}$ | —    | —                   | V             |
| Control Current                                          | —                   | —    | 1                   | $\mu\text{A}$ |

**Notes:**

1. Loss values are de-embedded from test board Loss (test board's Insertion Loss: 0.10dB @100MHz, 0.40dB @1200MHz, 0.55dB @2000MHz, 0.75dB @4000MHz).
2. Input IP3 and 1dB compression degrades below 1 MHz.
3. During turn-on and transition between attenuation states, device may draw up to 2mA.

**Switching Specifications**

| Parameter                                                  | Min. | Typ. | Max. | Units           |
|------------------------------------------------------------|------|------|------|-----------------|
| Switching Speed, 50% Control to 0.5dB of Attenuation Value | —    | 1.0  | —    | $\mu\text{Sec}$ |
| Switching Control Frequency                                | —    | —    | 25   | KHz             |

**Absolute Maximum Ratings**

| Parameter             | Ratings                               |
|-----------------------|---------------------------------------|
| Operating Temperature | -40°C to 85°C                         |
| Storage Temperature   | -55°C to 100°C                        |
| $V_{DD}$              | -0.3V Min., 4V Max.                   |
| Voltage on any input  | -0.3V Min., $V_{DD}+0.3\text{V}$ Max. |
| ESD, HBM              | 500V                                  |
| ESD, MM               | 100V                                  |
| Input Power           | +24dBm                                |

Permanent damage may occur if any of these limits are exceeded.

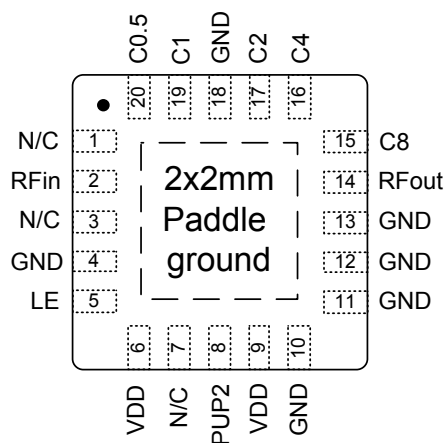
## Pin Description

| Function        | Pin Number | Description                         |
|-----------------|------------|-------------------------------------|
| N/C             | 1          | Not connected (Note 3)              |
| RF in           | 2          | RF in port (Note 1)                 |
| N/C             | 3          | Not connected (Note 3)              |
| GND             | 4          | Ground connection                   |
| LE              | 5          | Latch Enable Input (Note 2)         |
| V <sub>DD</sub> | 6          | Power Supply                        |
| N/C             | 7          | Not connected                       |
| PUP2            | 8          | Power up selection bit              |
| V <sub>DD</sub> | 9          | Power supply                        |
| GND             | 10         | Ground connection                   |
| GND             | 11         | Ground connection                   |
| GND             | 12         | Ground connection (Note 5)          |
| GND             | 13         | Ground connection                   |
| RF out          | 14         | RF out port (Note 1)                |
| C8              | 15         | Control for attenuation bit, 8 dB   |
| C4              | 16         | Control for attenuation bit, 4 dB   |
| C2              | 17         | Control for attenuation bit, 2 dB   |
| GND             | 18         | Ground Connection                   |
| C1              | 19         | Control for attenuation bit, 1 dB   |
| C0.5            | 20         | Control for attenuation bit, 0.5 dB |
| GND             | Paddle     | Paddle ground (Note 4)              |

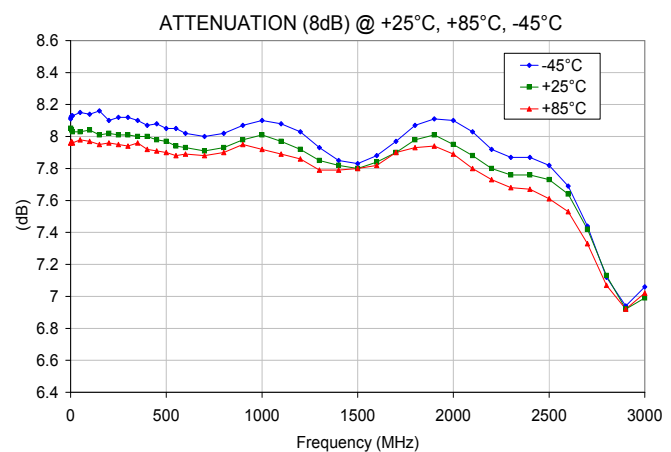
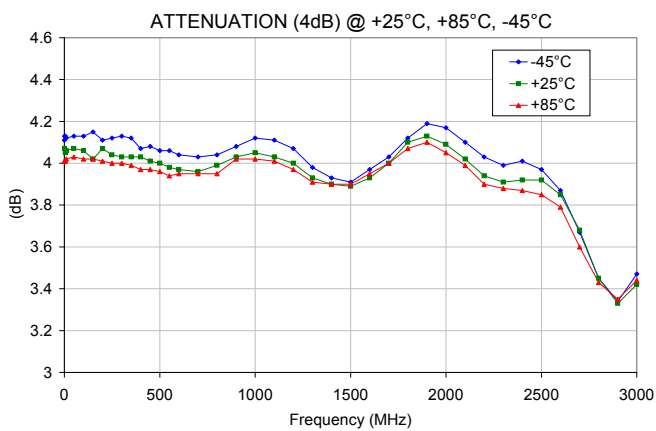
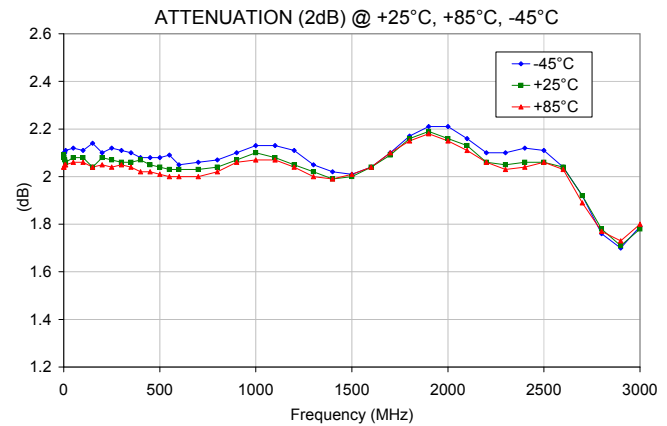
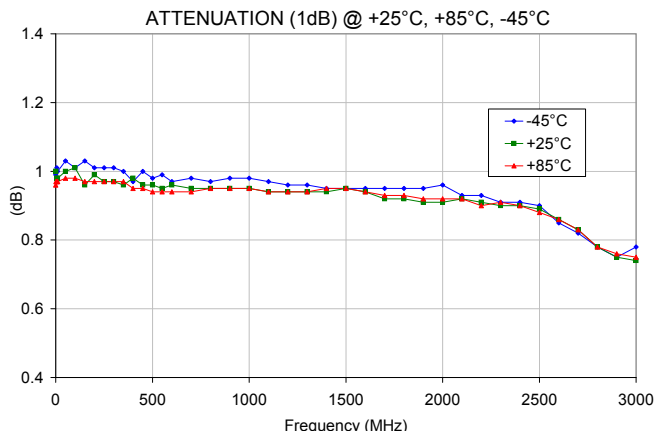
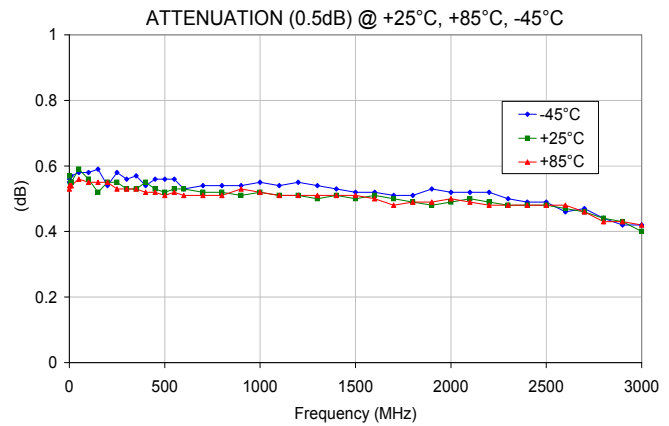
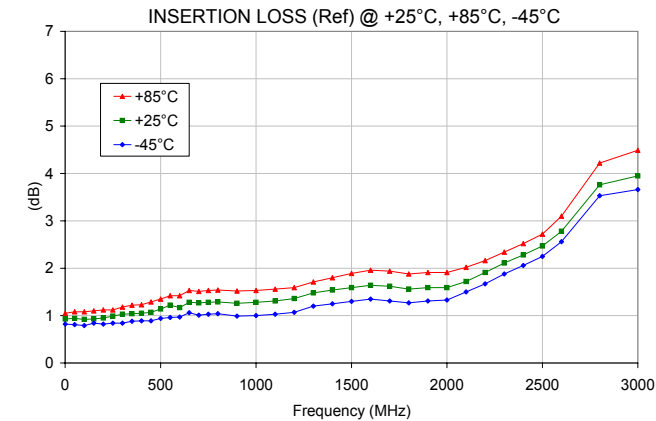
## Notes:

- Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.
- Latch Enable (LE) has an internal 100KΩ resistor to V<sub>DD</sub>.
- Place a 10KΩ resistor to GND.
- The exposed solder pad on the bottom of the package (See Pin Configuration) must be grounded for proper device operation.
- Ground must be less than 80 mil (0.08") from Pin 12 for proper device operation.

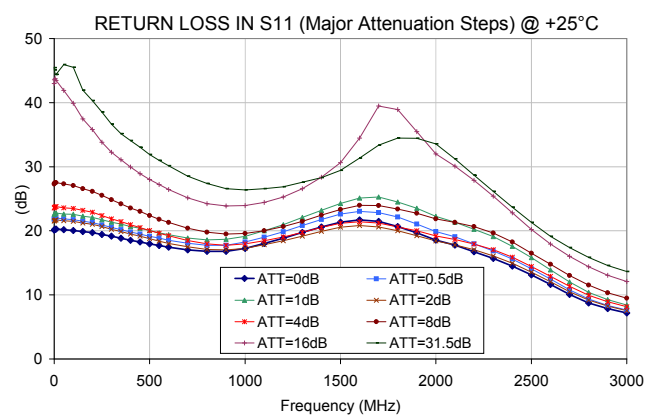
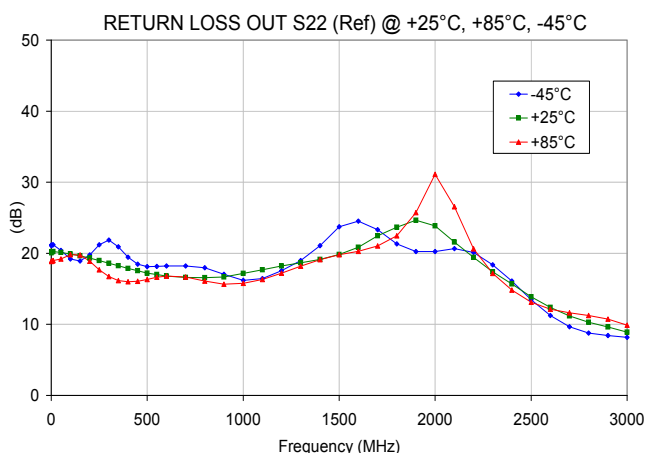
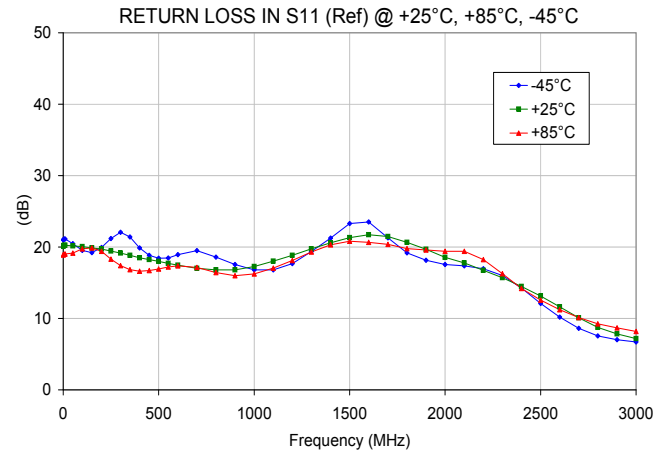
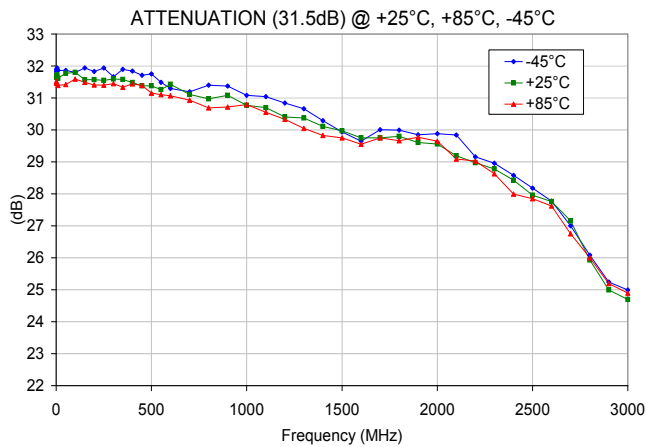
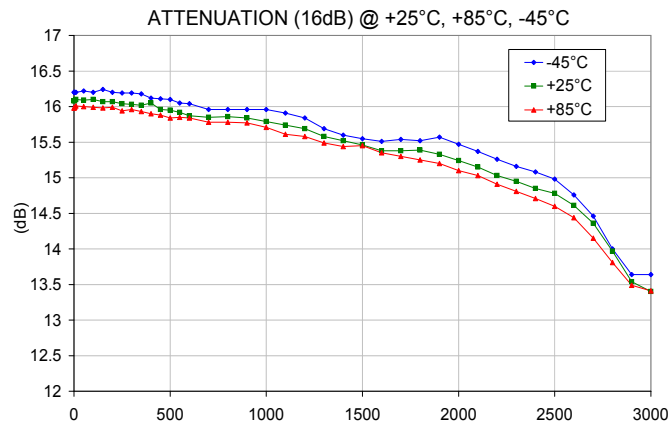
## Pin Configuration (Top View)



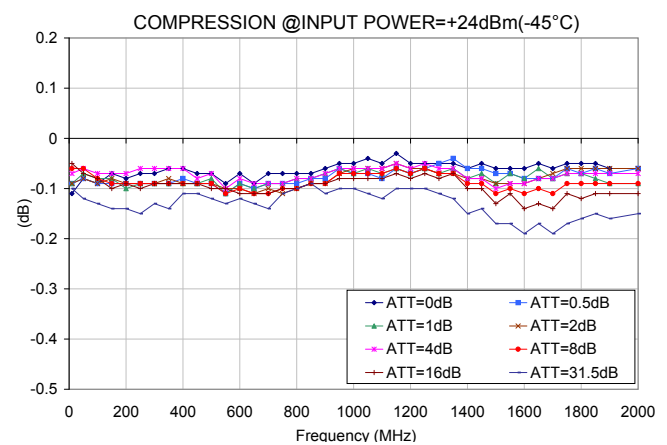
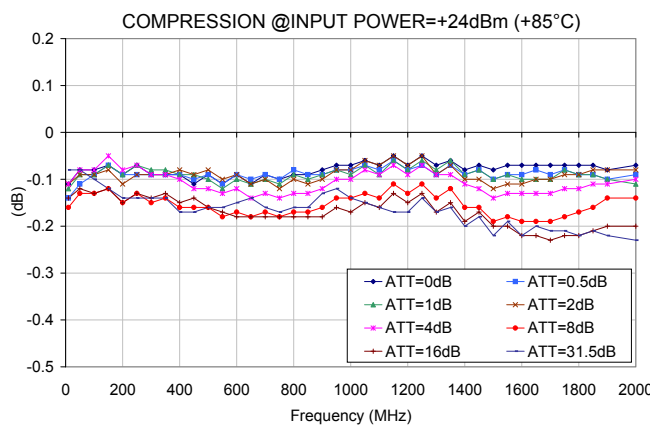
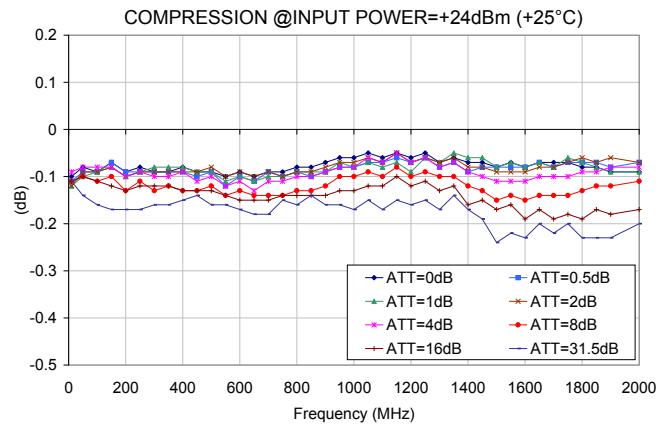
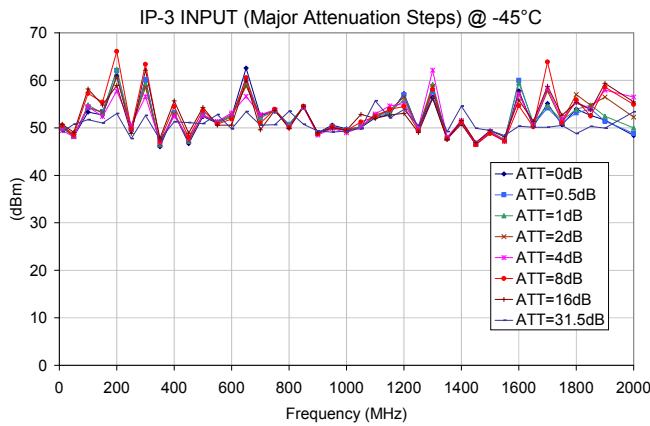
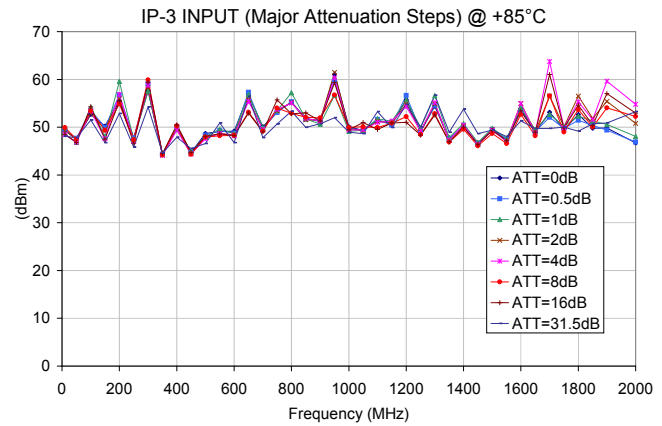
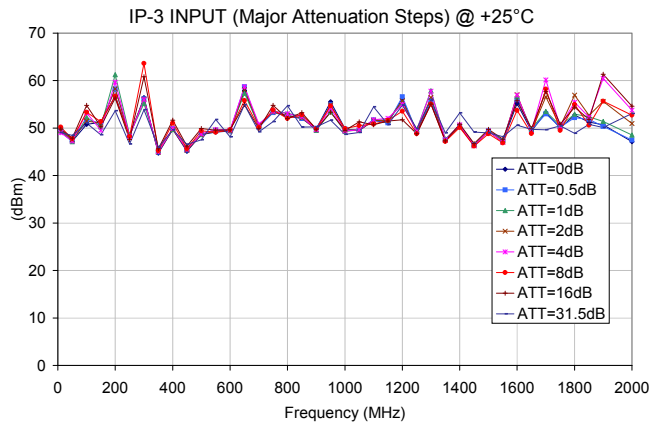
## Typical Performance Curves



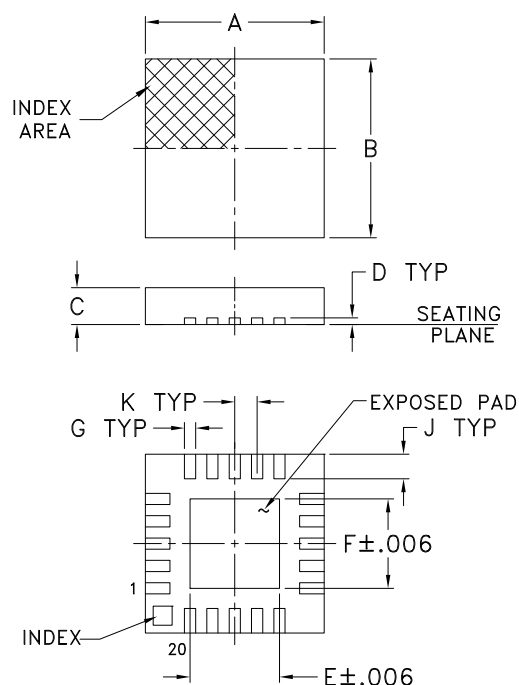
## Typical Performance Curves



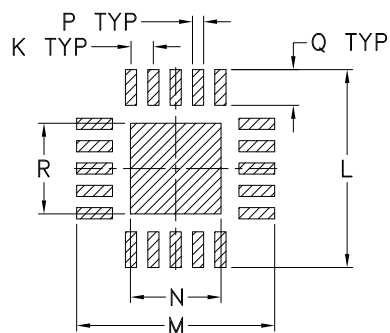
## Typical Performance Curves



## Outline Drawing (DG983-1)

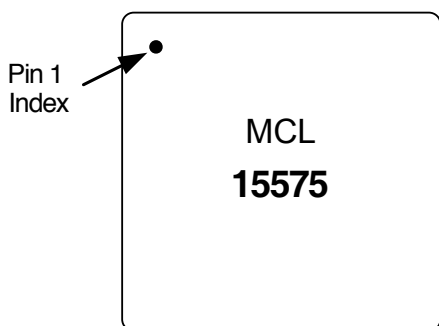


## PCB Land Pattern



Suggested Layout,  
Tolerance to be within  $\pm.002$

## Device Marking

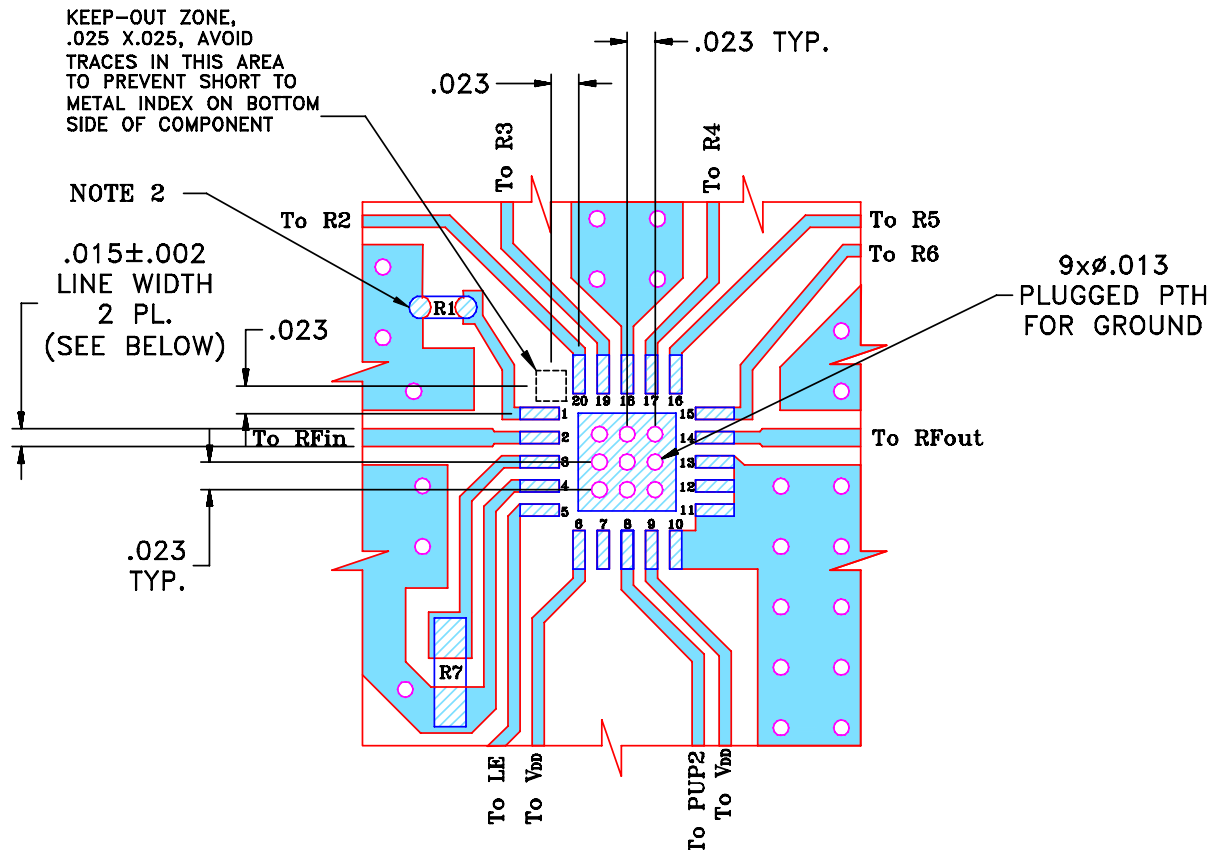


## Outline Dimensions (inch/mm)

| A    | B    | C    | D    | E    | F    | G    | H | J    | K    | L    | M    | N    | P    | Q    | R    | WT. GRAMS |
|------|------|------|------|------|------|------|---|------|------|------|------|------|------|------|------|-----------|
| .157 | .157 | .035 | .008 | .081 | .081 | .010 | — | .022 | .020 | .177 | .177 | .081 | .010 | .032 | .081 | .04       |
| 4.00 | 4.00 | 0.90 | 0.20 | 2.06 | 2.06 | 0.25 | — | 0.56 | 0.50 | 4.50 | 4.50 | 2.06 | 0.25 | 0.81 | 2.06 |           |

**Suggested Layout for PCB Design (PL-201)**

The suggested Layout shows only the footprint area of the DAT, and the components located near this area (i.e.: R1, R7). For the complete Layout, see photo and schematic diagram on page 11 of 12.

**NOTES:**

1. TRACE WIDTH IS SHOWN FOR FR4 WITH DIELECTRIC THICKNESS. .025"±.002". COPPER: 1/2 OZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.
2. 0603, 0402 SIZES CHIP FOOT PRINTS SHOWN FOR REFERENCE, VALUES OF RESISTORS WILL VARY BASED ON APPLICATION.
3. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.

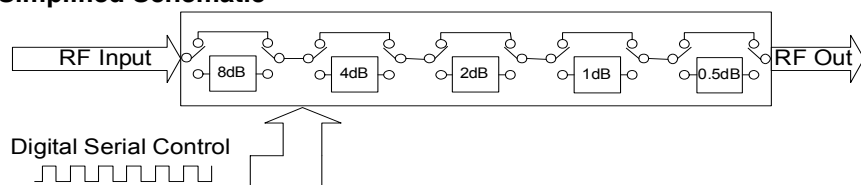


DENOTES PCB COPPER LAYOUT WITH SMOBC (SOLDER MASK OVER BARE COPPER)



DENOTES COPPER LAND PATTERN FREE OF SOLDERMASK

## Simplified Schematic



The DAT-15575-PP+ Parallel interface consists of 5 control bits that select the desired attenuation state, as shown in **Table 1**: Truth Table

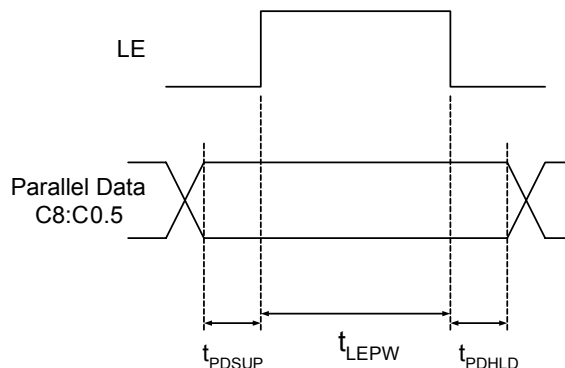
| Table 1. Truth Table                                                   |    |    |    |    |      |
|------------------------------------------------------------------------|----|----|----|----|------|
| Attenuation State                                                      | C8 | C4 | C2 | C1 | C0.5 |
| Reference                                                              | 0  | 0  | 0  | 0  | 0    |
| 0.5 (dB)                                                               | 0  | 0  | 0  | 0  | 1    |
| 1 (dB)                                                                 | 0  | 0  | 0  | 1  | 0    |
| 2 (dB)                                                                 | 0  | 0  | 1  | 0  | 0    |
| 4 (dB)                                                                 | 0  | 1  | 0  | 0  | 0    |
| 8 (dB)                                                                 | 1  | 0  | 0  | 0  | 0    |
| 15.5 (dB)                                                              | 1  | 1  | 1  | 1  | 1    |
| Note: Not all 32 possible combinations of C0.5 - C8 are shown in table |    |    |    |    |      |

The parallel interface timing requirements are defined by Figure 1 (Parallel Interface Timing Diagram) and Table 2 (Parallel Interface AC Characteristics), and switching speed.

For latched parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per Figure 1) to latch new attenuation into device.

For direct parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardware, switches, or jumpers)

**Figure 1: Parallel Interface Timing Diagram**



| Table 2. Parallel Interface AC Characteristics |                                                 |      |      |       |
|------------------------------------------------|-------------------------------------------------|------|------|-------|
| Symbol                                         | Parameter                                       | Min. | Max. | Units |
| $t_{LEPW}$                                     | LE minimum pulse width                          | 10   |      | ns    |
| $t_{PDSUP}$                                    | data set-up time before clock rising edge of LE | 10   |      | ns    |
| $t_{PDHL}$                                     | data hold time after clock falling edge of LE   | 10   |      | ns    |

Pin 1 must always be low to prevent the attenuator from entering an unknown state.

### Power-up Control Settings

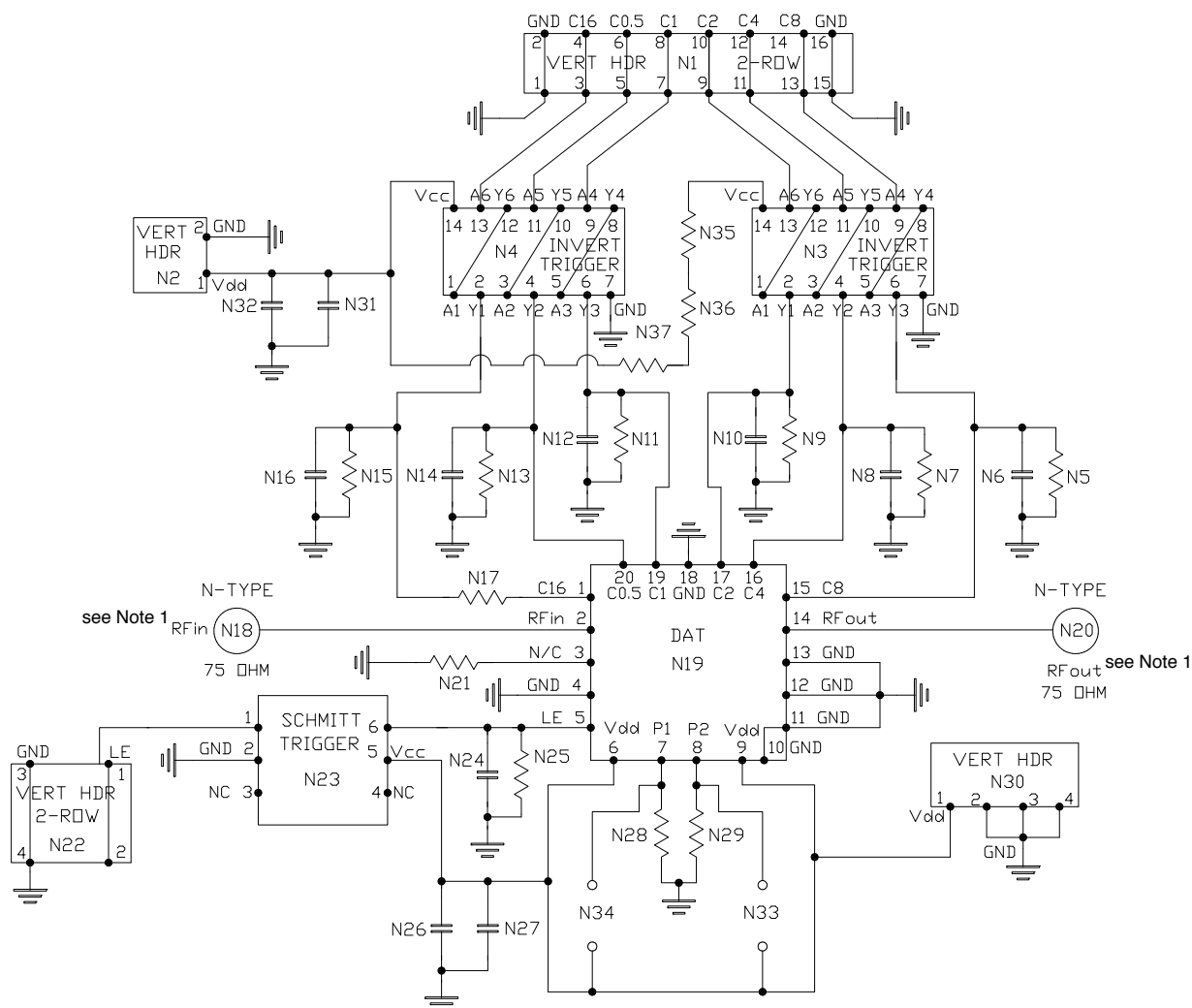
The DAT-15575-PP+ always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial parallel control word is provided.

When the attenuator powers up with LE=0, the control bits are automatically set to one of two possible values. These two values are selected by the power-up control bit, PUP2, as shown in Table 3: (Power-Up Truth Table, Parallel Mode).

| Table 3. Power-Up Truth Table, Parallel Mode                                                      |            |    |
|---------------------------------------------------------------------------------------------------|------------|----|
| Attenuation State                                                                                 | PUP2       | LE |
| Reference                                                                                         | 0          | 0  |
| 8 (dB)                                                                                            | 1          | 0  |
| Defined by C0.5-C8<br>(See Table 1-Truth Table)                                                   | X (Note 1) | 1  |
| Note 1: PUP2 Connection may be 0, 1, GROUND, or not connect, without effect on attenuation state. |            |    |

Power-Up with LE=1 provides normal parallel operation with C0.5-C8, and PUP2 is not active.

## TB-337 Evaluation Schematic Diagram



Note 1: Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.

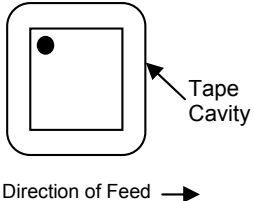
| Bill of Materials                          |                                        |
|--------------------------------------------|----------------------------------------|
| N5, N7, N9, N11, N13, N15, N21 & N25       | Resistor 0603 10 KOhm +/- 1%           |
| N28 & N29                                  | Resistor 0603 475 Ohm +/- 1%           |
| N35-N37                                    | Resistor 0603 0 Ohm                    |
| N17                                        | Resistor 0402 10 KOhm +/- 1%           |
| N6, N8, N10, N12, N14, N16, N24, N26 & N32 | NPO Capacitor 0603 100pF +/- 5%        |
| N27 & N31                                  | Tantalum Capacitor 0805 100nF +/- 10%  |
| N3 & N4                                    | Hex Invert Schmitt Trigger MSL1        |
| N23                                        | Dual Schmitt Trigger Buffer SC-70 MSL1 |



**TB-337**

## Tape and Reel Packaging Information

Table T&amp;R

| TR No. | No. of Devices                               | Reel Size | Tape Width | Pitch | Unit Orientation                                                                    |
|--------|----------------------------------------------|-----------|------------|-------|-------------------------------------------------------------------------------------|
| F87    | Small quantity standards<br>20, 50, 100, 200 | 7 inch    | 12 mm      | 8 mm  |  |
|        | 3000<br>(Standard)                           | 13 inch   |            |       |                                                                                     |

## Additional Notes

- A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
- B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
- C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at [www.minicircuits.com/MCLStore/terms.jsp](http://www.minicircuits.com/MCLStore/terms.jsp)